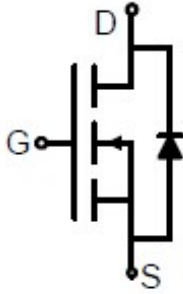
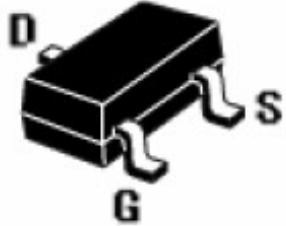


<p><b>Description</b></p> <p>The G1002L uses advanced trench technology and design to provide excellent <math>R_{DS(ON)}</math> with low gate charge. It can be used in a wide variety of applications.</p> <p><b>General Features</b></p> <ul style="list-style-type: none"> <li>●</li> </ul> <table border="1" style="width: 100%; border-collapse: collapse; margin-bottom: 10px;"> <tr> <td style="padding: 5px;"><math>V_{DSS}</math></td> <td style="padding: 5px;"><math>R_{DS(ON)}</math> @ 10V (typ)</td> <td style="padding: 5px;"><math>I_D</math></td> </tr> <tr> <td style="padding: 5px;">100V</td> <td style="padding: 5px;">180mΩ</td> <td style="padding: 5px;">2A</td> </tr> </table> <ul style="list-style-type: none"> <li>● High density cell design for ultra low <math>R_{dson}</math></li> <li>● Fully characterized avalanche voltage and current</li> <li>● Excellent package for good heat dissipation</li> </ul> <p><b>Application</b></p> <ul style="list-style-type: none"> <li>● Power switching application</li> <li>● Hard switched and high frequency circuits</li> <li>● Uninterruptible power supply</li> </ul>	$V_{DSS}$	$R_{DS(ON)}$ @ 10V (typ)	$I_D$	100V	180mΩ	2A	<div style="text-align: center;">  <p><b>Schematic diagram</b></p>  <p><b>SOT23-3L</b></p> </div>
$V_{DSS}$	$R_{DS(ON)}$ @ 10V (typ)	$I_D$					
100V	180mΩ	2A					

**Absolute Maximum Ratings ( $T_A=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	2	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	5	A
Maximum Power Dissipation	$P_D$	1.1	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	120	$^{\circ}C/W$
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**Electrical Characteristics ( $T_A=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$

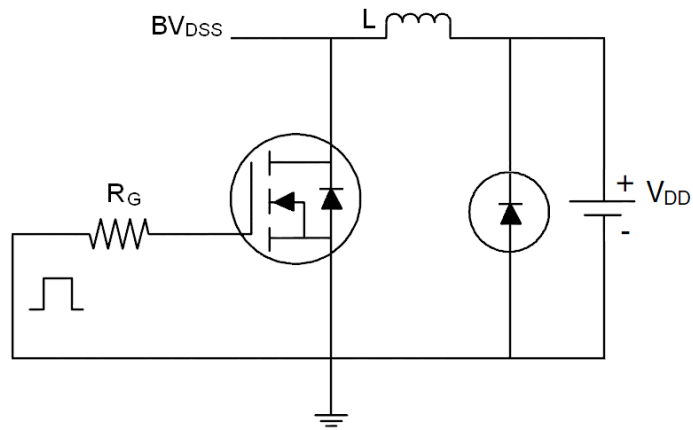
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.8	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=1A$	-	180	250	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=1A$	1	-	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{ISS}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	190	-	PF
Output Capacitance	$C_{OSS}$		-	22	-	PF
Reverse Transfer Capacitance	$C_{RSS}$		-	13	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=1.3A, R_L=39\Omega$ $V_{GS}=10V, R_G=1\Omega$	-	6	-	nS
Turn-on Rise Time	$t_r$		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	10	-	nS
Turn-Off Fall Time	$t_f$		-	6	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=1.3A,$ $V_{GS}=10V$	-	5.2	-	nC
Gate-Source Charge	$Q_{gs}$		-	0.75	-	nC
Gate-Drain Charge	$Q_{gd}$		-	1.4	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=1.3A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	2	A

## Notes:

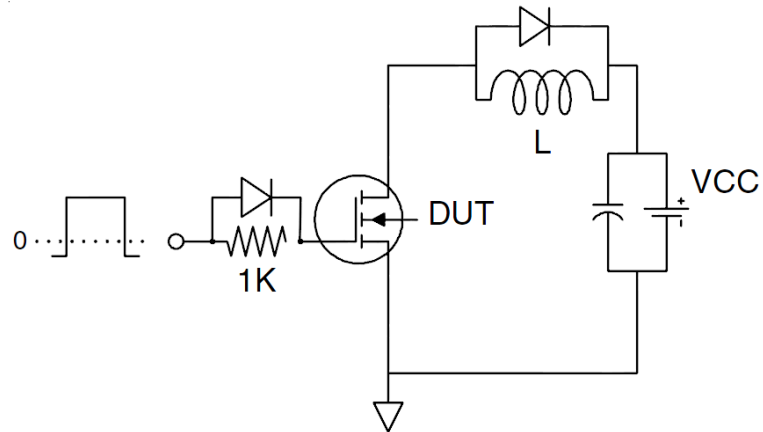
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

## Test Circuit

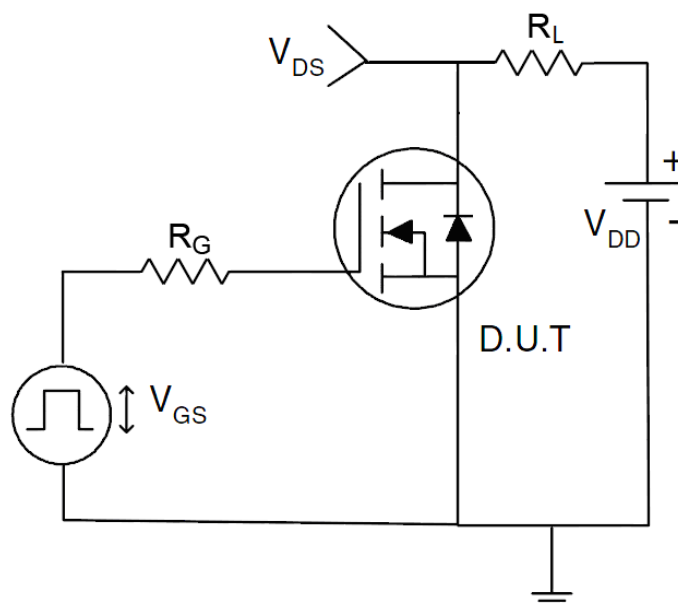
### 1) $E_{AS}$ test circuit



### 2) Gate charge test circuit



### 3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

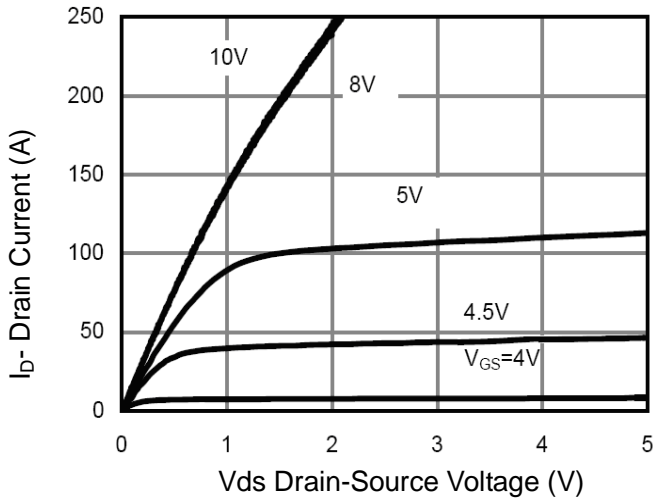


Figure 1 Output Characteristics

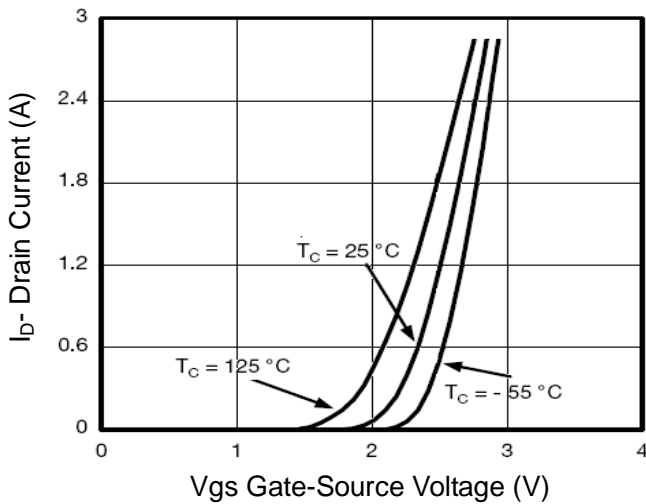


Figure 2 Transfer Characteristics

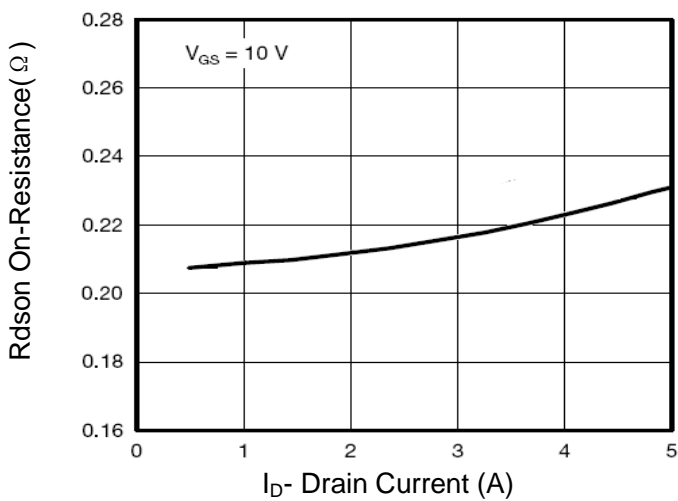


Figure 3 Rdson- Drain Current

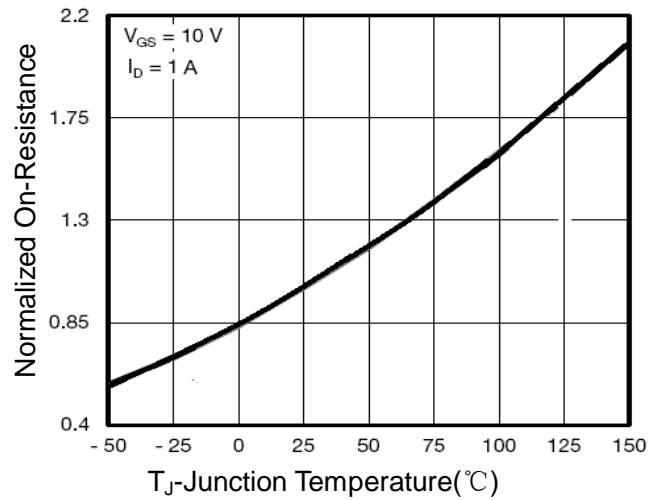


Figure 4 Rdson-Junction Temperature

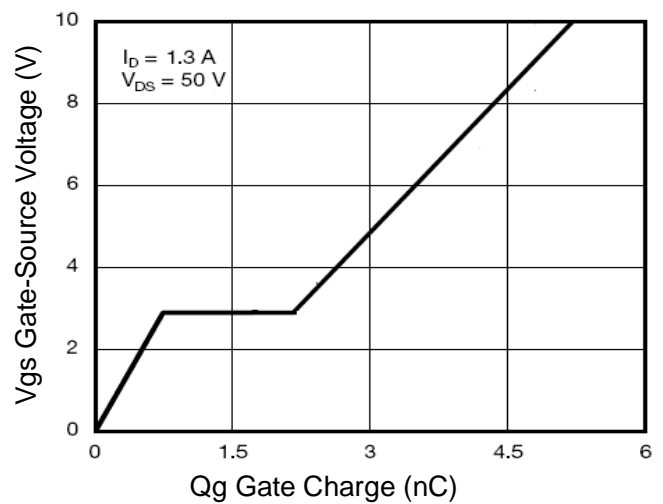


Figure 5 Gate Charge

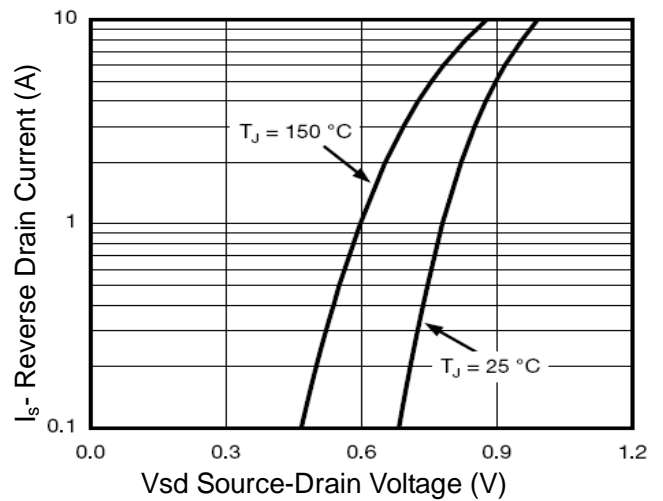


Figure 6 Source- Drain Diode Forward

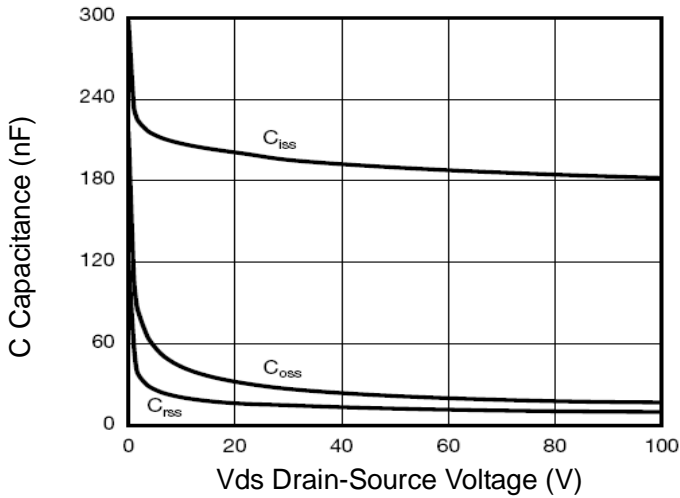


Figure 7 Capacitance vs Vds

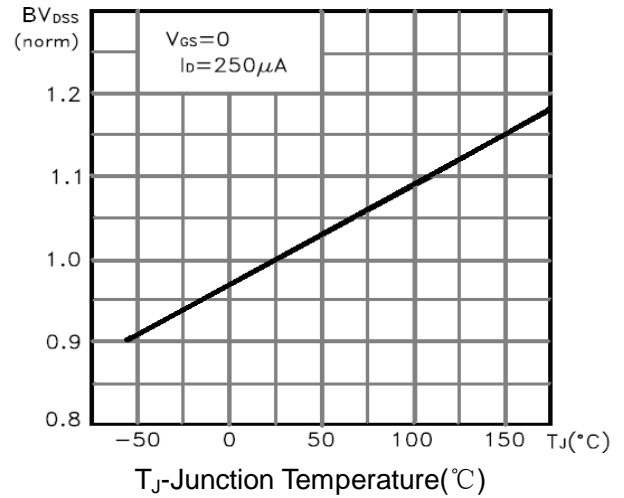


Figure 9  $BV_{DSS}$  vs Junction Temperature

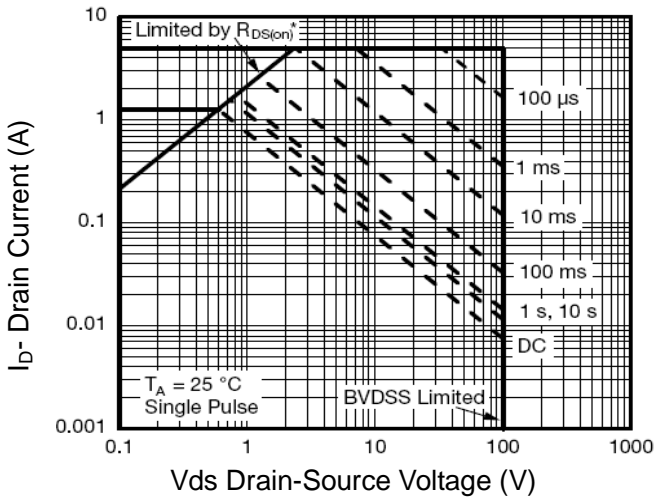


Figure 8 Safe Operation Area

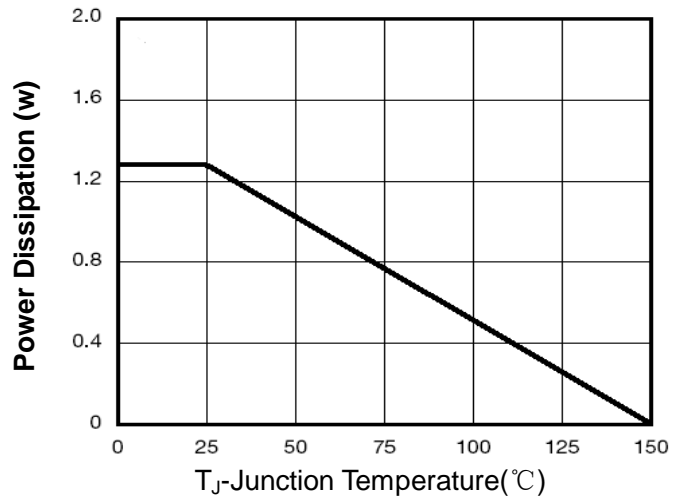


Figure 10 Power De-rating

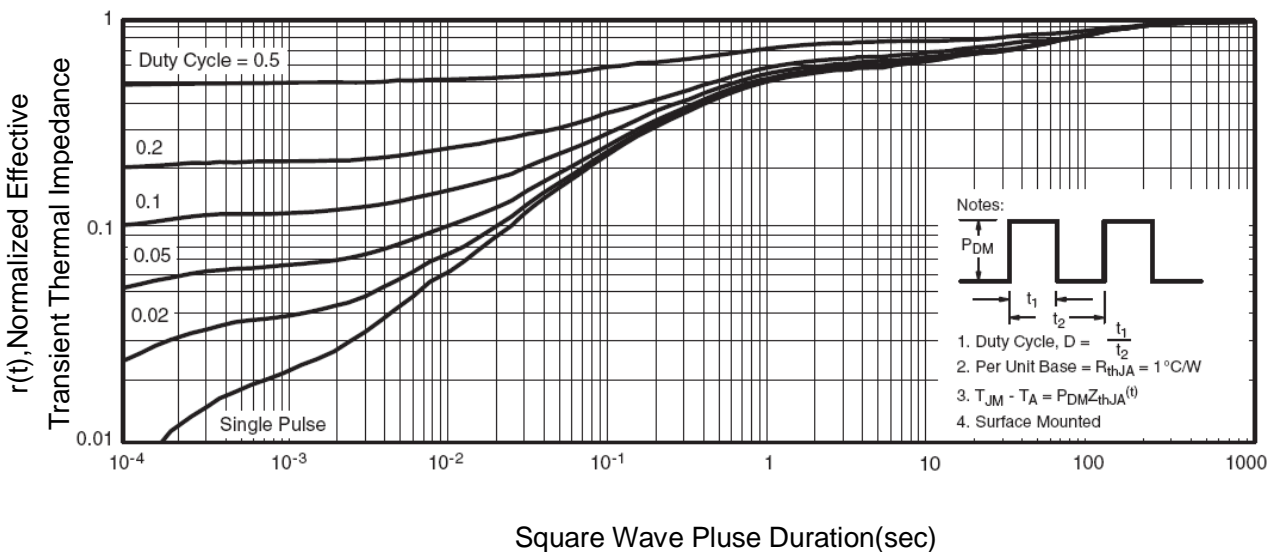


Figure 11 Normalized Maximum Transient Thermal Impedance